DOCKET NO. 02-5624 Express Mailing Label No. EU881765873US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Byung-Sung Kwak, Jayanthi Pallinti, and William Barth	)	
Filed: Herewith	)	Group Art Unit: Unknown
Serial Number: Unknown	)	Examiner: Unknown
Title: "Process for Reducing Impurity Levels, Stress, and Resistivity, and Increasing Grain Size of Copper Filler in Trenches and Vias of Integrated Circuit Structures to Enhance Electrical Performance of Copper Filler"	)	

FIRST INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.56

Honorable Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

September 30, 2003

Sir:

Pursuant to 37 CFR 1.56, Applicants hereby submit the references listed on the attached form PTO-1449 (modified), which may be relevant to this case. Copies of each of the references are enclosed.

Respectfully submitted,

By: John P. Taylor

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Attorney for Applicants
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Legal Department - IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035

FORM PTO-1449 (Modified) U.S. Department of Commerce, Patent and Trademark Office	Docket No. 02-5624	Serial No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicants Byung-Sung Kwak et al.	
	Filing Date Herewith	Group Unknown

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,874,367	2/23/99	Dobson	438	787	
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	Bothra, S., et al., "Integration of 0.25 μm Three and Five Level Interconnect System for High Performance ASIC", 1997 Proceedings Fourteenth International VMIC Conference, Santa Clara, CA, June 10-12, 1997, pp.43-48.
	AS	Brongersma, S.H., et al., 'Non-Correlated Behavior of Sheet Resistance and Stress During Self-Annealing of Electroplated Copper", IITC, 1999, pp.290-292.
	AT	Dobson, C.D., et al., "Advanced SiO_2 Planarization Using Silane and H_2O_2", Semiconductor International, December 1994, pp. 85-88.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance *and* not considered. Include copy of this form with your communication to applicant.

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	BA						
	BB						
	BC						
	BD						
	BE						
	BF						
	BG						
	BH						
	BI						
	BJ						
	BK						

Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	BL							
	BM							
	BN							
	BO							
	BP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	BR	Hau-Riege, Stefan P., Handbook entitled "Copper Interconnect Technology", University of California-Berkeley Extension Course, April, 2002, pp. 129-137.
	BS	Kittel, Charles, Introduction to Solid State Physics, 6th ed., New York: John Wiley & Sons, 1986, pp. 143, 145.
	BT	McClatchie, S., et al., "Low Dielectric Constant Oxide Films Deposited Using CVD Techniques", 1998 Proceedings Fourth International DUMIC Conference, February 16-17, 1998, pp. 311-318.

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	CA						
	CB						
	CC						
	CD						
	CE						
	CF						
	CG						
	CH						
	CI						
	CJ						
	CK						

Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	CL							
	CM							
	CN							
	CO							
	CP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	CR	Peters, Laura, "Low-k Dielectrics: Will Spin-On or CVD Prevail?", Semiconductor International, Vol. 23, No. 6, June, 2000, pp. 108-110, 114, 116, 118, 122, and 124.
	CS	Peters, Laura, "Pursuing the Perfect Low-k Dielectric", Semiconductor International, Vol. 21, No. 10, September, 1998, pp. 64-66, 68, 70, 72, and 74.
	CT	Ramanan, V.R.V., et al., "Crystallization Kinetics in Fe-B-Si Metallic Glasses", J. Appl. Phys., Vol. 53, No. 3, March, 1982, pp. 2273-2275.

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	DA						
	DB						
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	DD						
	DE						
	DF						
	DG						
	DH						
	DI						
	DJ						
	DK						

Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	DL							
	DM							
	DN							
	DO							
	DP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	DR	Ritzdorf, T., et al., "Comparative Investigation of Plating Conditions on Self-Annealing of Electrochemically Deposited Copper Films", IITC, 1999, pp. 287-289.
	DS	Rossnagel, S.M., et al., "From PVD to CVD to ALD for Interconnects and Related Applications", IITC, 2001, p. 2.
	DT	

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